EENG 284

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Digital Design Lab

Lab 1

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Introduction to CAD tools and Verilog

Lab Solutions

# Part 1: Setting up a project in Quartus and running a testbench.

This is the timing diagram for an AND gate.

Graphical user interface

Description automatically generated

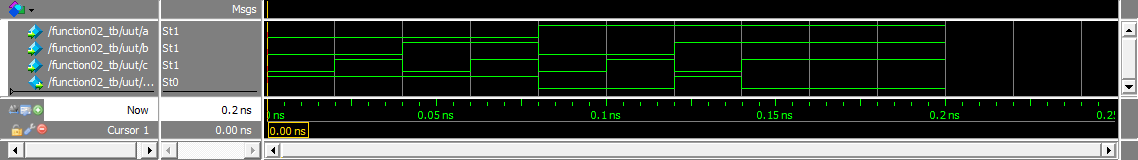
# Part 2: Symbolic to Verilog , Timing Diagram, Truth Table.

Write Verilog code to realize the function *f02 = a’ + bc’*

**Part 2:**  Step 4 Verilog code for *f02*

assign f02 = (~ a) | (b & ~c);

**Part 2:**  Step 7 Timing diagram of *f02*

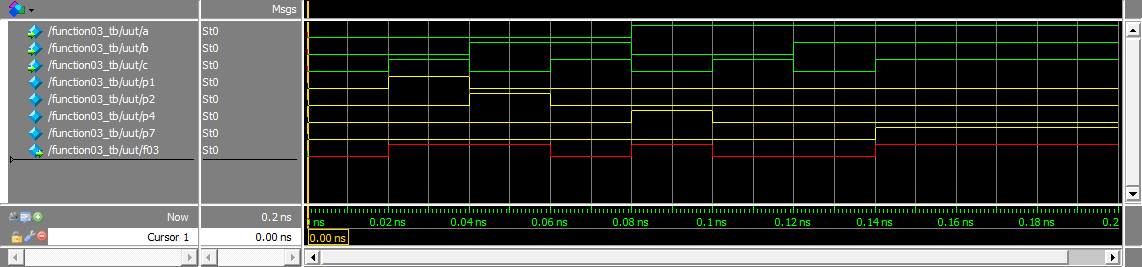


**Part 2:**  Step 8 Truth table of *f02*

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | c | f02 |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

# Part 3: Verilog to Symbolic, Truth Table, Circuit Diagram

**Part 3:**  Step 6 Timing diagram of *f03*

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**Part 3:**  Step 8 Truth table of *f03*

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | c | f03 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

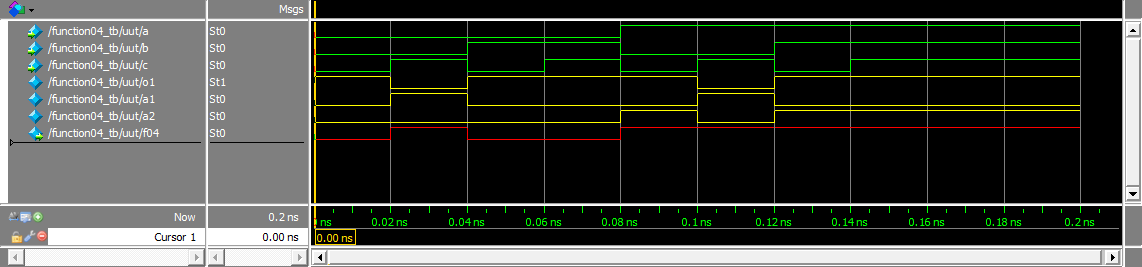
**Part 3:**  Step 9 Circuit Diagram of *f03*

To Be Done

**Part 3:**  Step 10 Symbolic form of *f03*

f03 = a’\*b’\*c + a’\*b\*c’ + a\*b’\*c’ + a\*b\*c

**Part 4: Circuit Diagram to Verilog, Symbolic, Truth Table**

**Part 4:**  Step 6 Timing diagram of *f04*

**Part 4:**  Step 8 Truth table of *f04*

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | c | f04 |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**Part 4:**  Step 9 Just the 4 Verilog assign statement for *o1*, *a1*, *a2*, and *f04*.

assign o1 = b | ~c;

assign a1 = ~b & c;

assign a2 = o1 & a;

assign f04 = a1 | a2;